UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,492	02/11/2002	Samantha J. Edirisooriya	30320/37804	6018

7590 05/21/2004

JAMES F. GOEDKEN
GROSSMAN & FLIGHT, LLC
20 NORTH WACKER DRIVE
SUITE 4220
CHICAGO, IL 60606

EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,492	EDIRISOORIYA ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-16* is/are allowed.

6)☒ Claim(s) *1-7,10-13,17-25 and 28-32* is/are rejected.

7)☒ Claim(s) *8,9,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on June 13, 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the Examiner.

Claim Objections

Claims 19-23 are objected to because of the following informalities:

Regarding claim 19, the claim recites "...a main memory operatively connected to the first microprocessor and the second microprocessor..." (lines 1-3). Parent claim 17 had previously recited "a main memory coupled to the first microprocessor and the second microprocessor" in lines 5-6. The Examiner believes that the instance of "a main memory" in claim 19 is directed to the "a main memory" of claim 17, and the Examiner will interpret the limitations of claim 19 as such. The Examiner encourages the Applicant to replace the second instance of "a" in line 1 of claim 19 with –the— in order to facilitate proper antecedent basis.

Claims 20-23 are objected to as being dependent upon an objected claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 10-13, 17-19, 24, 25, and 28-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang (US# 6,519,685).

Regarding claim 1, Chang teaches **cache intervention** (the updating of modified data) by **reading a memory block** (line) **from main memory into the cache** of caching agent #1 **and tagging** (marking) **the line as non-modified** (Exclusive) (col. 8, line 65 – col. 9, line 4; col. 4, lines 46-53). **Caching agent #2 performs a memory read operation that hits caching agent #1's data**, whereupon **agent #1 responds, due to the detection, with a response to agent #2** (Shared Snoop). **Agent #1 is responsible for providing the memory block (line) to Agent #2** (col. 9, lines 49-53 & 66 – col. 10, line 4) due to the non-modified (Exclusive) state of the data.

Regarding claim 2, and as recited above, Chang teaches that the **loading of the cache block (line) into the cache from the main memory includes tagging the line as Exclusive** (col. 6, lines 36-39; col. 8, line 65 – col. 9).

Regarding claim 3, according to the claim limitations the "tagging" operation is not required to immediately follow the "reading" operation. As such, operations may have occurred before the claimed "tagging" operation, such as first tagging the loaded memory block (line) as "Exclusive", followed by the request from another agent (agent #2) for the "Exclusive" data. Chang teaches that the first agent will provide the memory block (line) to the another agent, at which point **the non-modified memory block (line) will be tagged as "Shared",** in accordance with the claim limitation. These steps are seen in column 9, lines 5-24, such that the operations following the "tagging" operation of the parent claim now correspond to caching agent #3.

Regarding claim 4, Chang teaches that the **memory block (line) of caching agents #1 and #2 are tagged as Shared in response to the read request** (col. 9, lines 9-14).

Regarding claim 5, Chang teaches **that detecting a read request includes snooping a bus** for the corresponding transaction data (col. 3, lines 29-35 & 58-67; col. 4, lines 32-36; col. 9, lines 5-14).

Regarding claim 6, Chang teaches that **a directory indicating the lines copied from main memory to a processors cache is used during the snoop read request by a second agent** (col. 10, lines 32-47 & line 66 – col. 11, line 17).

Regarding claim 7, Chang teaches **detecting a read request for the cache block (line) by a third cache (agent).** Both cache (agents) #1 and #2 hold the data in a non-modified state, and **the system of Chang determines (arbitrates) that caching agent #1 will supply the data to caching agent #3 due to the tagged state of the data in caching agent #1**. The **memory block (line) is copied to cache (agent) #3, which is required before the memory block (line) can be tagged as non-modified** (Shared) (col. 9, lines 15-24; col. 7, lines 8-22).

Regarding claim 10, Chang teaches that each "caching agent" has caching capabilities, such as a processor. Each processor is coupled to a cache as seen in Figure 1. Figure 1 also indicates that **multiple (first and second) processor's and their associated (first and second) caches are couple by a bus (108) (cache interconnect)**. A shared **main memory (106) is also coupled to the first and second processing "agents"** via the cache interconnect (bus) (108) and the unmarked bus between shared main memory (106) and cache interconnect (108) (col. 3, lines 28-35 & 45-49). This unmarked bus will now be referred to as the **main memory interconnect**.

Chang teaches **reading a memory block** (line) **from main memory into the cache** of caching agent #1 (**via main memory interconnect**; Fig. 1) **and tagging** (marking) **the line as** Exclusive (**non-modified**) (col. 8, line 65 – col. 9, line 4; col. 4, lines 46-53). **Caching agent #2 performs a memory read operation that hits**

caching agent #1's data, whereupon **agent #1 responds, due to the detection, with a response to agent #2** (Shared Snoop). **Agent #1 is responsible for providing the memory block (line) to Agent #2** (col. 9, lines 49-53 & 66 – col. 10, line 4) due to the non-modified (Exclusive) state of the data. Cache interconnect (bus) (108) is used to support the bus transactions and thus the movement of data between caches would inherently require moving the data **on the cache interconnect (bus)** (108).

Regarding claim 11, Chang teaches that **upon detection of a read request from caching agent #2 for a memory block (line) by caching agent #1**, the **memory block (line) of caching agent #1 is tagged as Shared in response to the read request of the second agent** (col. 9, lines 5-12).

Regarding claim 12, Chang teaches **that processing agent #1 detects a read request by snooping the cache interconnect (bus)** for the corresponding transaction data and responds to the request second processing agent (col. 4, lines 32-36; col. 9, lines 5-14).

Regarding claim 13, Chang teaches **detecting a read request for the cache block (line) by a third cache (agent).** Both cache (agents) #1 and #2 hold the data in a non-modified state, and **the system of Chang determines (arbitrates) that caching agent #1 will supply the data to caching agent #3 due to the tagged state of the data in caching agent #1 via cache interconnect (bus) (108).** The **memory block**

(line) is copied to cache (agent) #3, which is required before the memory block (line can be tagged as non-modified (Shared) (col. 9, lines 15-24; col. 7, lines 8-22).

Regarding claim 17, Chang teaches that each "caching agent" has caching capabilities, such as a processor. As seen in Figure 1, **a first microprocessor** [CPU 1] **includes a first cache** [cache 1] **and a second microprocessor** [CPU 2] **includes a second cache** [cache 2], **where the first cache stores a copy of a memory block** [cache line] **in a non-modified** [exclusive] **state** (col. 9, lines 1-2 & 7). **A main memory is coupled to the first microprocessor and second microprocessor** [shared main memory (106)]. **The first microprocessor is responsible for providing the memory block (line) to the second cache of the second microprocessor** (col. 9, line 66 – col. 10, line 4) **due to the non-modified** (Exclusive) **state of the data in the first cache of the first microprocessor**.

Regarding claim 18, Chang teaches that **the first microprocessor will supply the second cache with the second copy of the memory block** (cache line) **while the first memory block** (cache line) **is in one of an exclusive state** and a shared state (col. 10, lines 1-4).

Regarding claim 19, Chang teaches that a **main memory is connected to the first microprocessor and second microprocessor** [shared main memory (106)] **by a**

main memory bus [(108)]. The **first microprocessor will directly supply the second cache with the second copy of the memory block** (cache line) **while the first copy is in the non-modified** (exclusive) **state** without the use of the main memory (col. 9, lines 57-65).

Regarding claim 24, Chang teaches **storing a memory block** (cache line) **stored in a first cache** (of the snooping agent) **is in a shared**-respond **state** (col. 10, lines 25-31; col. 3, lines 29-36). The snooping agent **detects a read request associated with the memory block by an agent** [requesting agent] **associated with a second cache** [of the requesting agent] **while the memory block in the first cache** [of the snooping agent] **is in the shared**-respond **state**. The snooping agent is responsible for **copying the memory block from the first cache to the second cache in response to detecting the read request while the memory block in the first cache is in the shared state** (col. 10, lines 26-31).

Regarding claim 25, Chang teaches that if another cache has the memory block (cache line) in a shared state, this cache will not be responsible for supplying the data to the requestor (col. 8, lines 26-31). The cache with the data in the shared-respond state is required to supply the data to the requestor if more than one cache contain the memory block (col. 10, lines 26-31; col. 7, lines 8-13). Therefore, **a third cache** (such as cache N of CPU N; Fig. 1) **with the memory block** (cache line) **is prevented from copying the memory block** (cache line) **to the second cache** (requesting agent)

because the third cache has the memory block in a shared state and not a shared-respond state.

Regarding claim 28, Chang teaches **storing a first copy of a memory block** (line) **into the first cache** of caching agent #1 **in one of an exclusive state and a shared state** [here, in the exclusive state (col. 8, line 65 – col. 9, line 4; col. 4, lines 46-53)]. Agent #1 **detects a memory read request associated with the memory block** of agent #1 **by a second agent (#2) and associated second cache** (col. 9, lines 5-8). The first agent is responsible for **supplying the second cache with a second copy of the memory block (line) while the first copy of the memory block is in one of the exclusive state and shared state without accessing main memory** (col. 9, line 57 – col. 10, line 4;)

Regarding claim 29, Chang teaches **that detecting a read request includes snooping a bus** for the corresponding transaction data (col. 3, lines 29-35 & 58-67; col. 4, lines 32-36; col. 9, lines 5-14).

Regarding claim 30, Chang teaches that **a directory indicating the lines copied from main memory to a processors cache is used to detect the snoop read request by a second agent** (col. 10, lines 32-47 & line 66 – col. 11, line 17).

Regarding claim 31, Chang teaches that the first microprocessor will **directly supply the second cache with the second copy of the memory block** (cache line) **while the first copy is in the Exclusive** (non-modified) **state** (col. 9, lines 57-65).

Regarding claim 32, the snooping agent detects a read request associated with the memory block by an agent [requesting agent] associated with a second cache [of the requesting agent] while the memory block in the first cache [of the snooping agent] is in the shared-respond state. The snooping agent is responsible for **supplying the second cache with the second copy of the memory block while the memory block in the first cache is in the shared state** (col. 10, lines 26-31).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US# 6,519,685) as applied to claims 1-7, 10-13, 17-19, 24, 25, and 28-32 above, and further in view of O'Leary et al. (US# 5,867,162).

Regarding claim 20, the difference between the claimed subject matter and that of Chang, disclosed supra, is that claim 20 recites that a motherboard, hard drive and

graphics (display) card are each coupled to the first microprocessor. As seen in Figure 2, O'Leary et al. teaches that the **motherboard** (204) **is coupled to the CPU**, and that the hard drive (212) and graphics (display) card(210) are coupled to the motherboard, and thus **the hard drive and graphics card are coupled to the CPU** (col. 3, lines 1-3). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Chang and O'Leary et al. before him at the time the invention was made to modify the cache coherency system of Chang to include the microprocessor (CPU) coupled system components of a motherboard, disk drive and graphics card of O'Leary et al. because by coupling the motherboard, hard drive, and graphics card system components to the CPU, the CPU is able provide them with the necessary instructions and operations in order for the system components to operate.

Regarding claim 21, Chang teaches that **an output device** (CRT display) outputs data via the I/O unit, where the I/O unit **is coupled** (interconnected) **to a** first **processing unit** (col. 1, lines 16-21), and thus the output device is coupled to the first processing unit. Chang teaches that **an input device** (keyboard) inputs instructions via the I/O unit, where the I/O unit **is coupled** (interconnected) **to a** first **processing unit** (col. 1, lines 10-15), and thus the input device is coupled to the first processing unit.

Regarding claim 22, Chang teaches that **the input device comprises** at least one of **a keyboard**, a mouse, a track pad, an isopoint, a microphone, and a graphics tablet (col. 1, line 13).

Regarding claim 23, Chang teaches that **the output device comprises** at least one of **a display**, a printer, a modem, a network card, and a speaker (col. 1, lines 20-21).

Allowable Subject Matter

Claims 14-16 are allowed over the prior art of record.

Claims 8, 9, 26, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related cache coherency systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

May 12, 2004

Brian R. Peugh
Patent Examiner
Art Unit 2187